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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,534	02/06/2002	Ming Michael Li	97-P-149D1 (850063.518D1)	9996

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EXAMINER	
ANYA, IGWE U	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/068,534	LI, MING MICHAEL
	Examiner	Art Unit
	Igwe U. Anya	2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1 – 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Lur et al. (US Patent 5554566).

3. Lur et al. teach an integrated semiconductor device, comprising:

a semiconductor material substrate (1);

a polysilicon line (4) forming a polysilicon gate region of the device (fig. 4) said polysilicon line having micro-rough indentations (6B) on a top surface portion of the polysilicon line formed by chemical mechanical polishing using, a slurry solution having particles of a maximum size of less than one-half of a width of the polysilicon line;

a silicide film (5) comprising titanium silicide or titanium silicide/titanium nitride stack film covering said micro-rough top surface portion of the polysilicon line (col. 4 lines 38 – 41), said silicide film has an increased effective surface area (inherency of a rough topography);

a plurality of isolation areas (2);

a thin oxide film (3) between said polysilicon line and the substrate;

a plurality of patterned active regions (7) forming source and drain regions of the device positioned on the substrate and on opposite sides of said polysilicon line;

spacers (8) adjacent to the polysilicon gate region and lightly doped regions under said spacers and adjacent to said source and drain regions; and

a metallization structure (11) positioned on the silicide film for providing interconnection, and wherein said metallization structure comprises a multi-stack metal layer (col. col. 4 line 61 – col. 5 line 5).

4. Claims 1 – 6, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Jeng et al. (US Patent 5893751).

5. Jeng et al. teach an integrated semiconductor device, comprising:

a semiconductor material substrate (10);

a polysilicon line (16) forming a polysilicon gate region of the device (fig. 2D) said polysilicon line having micro-rough indentations (col. 3 lines 7 - 15) on a top surface portion of the polysilicon line formed by chemical mechanical polishing using, a slurry solution having particles of a maximum size of less than one-half of a width of the polysilicon line;

a silicide film (27) comprising titanium silicide or titanium silicide/titanium nitride stack film covering said micro-rough top surface portion of the polysilicon line (col. 3 lines 22 – 38), said silicide film has an increased effective surface area (inherency of a rough topography);

a plurality of isolation areas (12);

a thin oxide film (14) between said polysilicon line and the substrate;

a plurality of patterned active regions (20) forming source and drain regions of the device positioned on the substrate and on opposite sides of the polysilicon line;

spacers (18) adjacent to the polysilicon gate region and lightly doped regions under said spacers and adjacent to said source and drain regions; and

wherein the width of the polysilicon line is less than 0.1 micron in width (col. 1 lines 15 – 21, & col. 1 lines 62 – 67).

6. The limitation "a top surface treated by chemical mechanical polishing using a slurry solution having particles of a maximum size of less than one-half the width of the polysilicon line to form micro-rough indentations in the top surface" has not been given any patentable weight. The method of forming a device is not germane to the issue of patentability of the device itself.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 10 – 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeng et al. (US Patent 5893751) in view of Ishida (US Patent 5937325).

9. Jeng et al. teach the features previously outlined, but lack wherein the silicide film is formed to enter a C-49 phase and not a C-54 phase.

10. However, Ishida teaches a silicide film (68) on a polysilicon line (56), wherein the silicide film is formed to enter a C-49 phase and not a C-54 phase (col. 3 line 28 – col. 4 line 39) for below 0.25 microns polysilicon dimensions to ensure a conversion to lower resistivity. Ishida further teaches its use in LDD-type MOS.

11. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ishida and Jeng et al. and employ a C-49 phase, in below 0.25 microns dimension to ensure a conversion to lower resistivity.

12. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeng et al. (US Patent 5893751) in view of Ishida (US Patent 5937325), and further in view of Lur et al. (US Patent 5554566).

13. Jeng et al./Ishida reference teaches the features previously outlined, but lack a metallization structure positioned on the silicide film for providing interconnection, and wherein said metallization structure comprises a multi-stack metal layer.

14. However, Lur et al. teach a metallization structure (11) positioned on the silicide film for providing interconnection, and wherein said metallization structure comprises a multi-stack metal layer (col. col. 4 line 61 – col. 5 line 5).

15. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Lur et al. into the Jeng et al./Ishida reference to position a multi-stack metal layer on the silicide layer to provide interconnection.

16. Prior art made of record and not relied upon, considered pertinent to applicant's disclosure include Gardner et al. (US Patent 5904529), Nasr (US Patent 5563096), McNeil et al. (US Patent 6242333), and Pierce (US Patent 5422289).

Remarks

17. Applicant's arguments filed January 4, 2005 have been fully considered but they are not persuasive. The method of forming a device is not germane to the issue of patentability of the device itself. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

18. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Igwe U. Anya whose telephone number is (571) 272-1887. The examiner can normally be reached on M - F 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Igwe U. Anya
Examiner
Art Unit 2891

IA

April 2, 2005

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER